amp inc
Memory and Storage Solutions for today's world
Accelerated Memory Production, Inc.

pSLC SD Card, 3.0, 16GB

Overview

Capacity = pSLC: 16GB	**Advanced Flash Management** Static and Dynamic Wear Leveling Bad Block Management SMART Function[Noted3] Auto-Read Refresh PPMS Embedded Mode
Flash Type= Toshiba 15nm MLC[Note1]	
Bus Speed Mode and Speed Class= UHS-I and Class 6/ 10	
Power Consumption[Note1] Power Up Current < 250uA Standby Current < 1mA Read Current <400mA Write Current <400mA	**Temperature Range** **Operation=** -25°C ~ 85°C **Storage=** -25°C ~ 85°C
Performance Read: Up to 95 MB/s Write: Up to 90 MB/s	**Supply Volta ge 2.7 ~ 3.6V**
	Write Protect w ith Mechanical Switch
CPRM (Content Protection for Recordable Media)	**RoHS compliant**
MTBF= More than 3,000,000 hours	**EMI compliant**

Notes:

1. Pseudo SLC can be considered as an extended version of MLC. Please see "1.2.8 Pseudo SLC (pSLC)" for details.
2. Please see "5.1 Power Consumption" for details.
3. This function is enabled by customer requirement and please see "1.2.4 Smart Function" for details.

Performance Overview

Capacity	Class	UHS-I	Controller	Flash			HDBenchWINXP (@1000MB) Kbytes		TestMetrix Test Test 500MB	
				Density	Process	Bit-percell	Read (KB/s)	Write (KB/s)	Read (KB/s)	Write (KB/s)
16GB	CL10	UHS-I (Grade 3)	PS8210	64Gb*4	15nm	Ultra MLC	93,610	86,340	99.50	91.91

Part Number	Capacity
AMPSD016G3S-00ES4YC-3P	16GB

1. INTRODUCTION

1.1. General Description

The pSLC Secure Digital Memory Card V 3.0 is fully compliant with the standards released by the SD Card Association. The Command List supports [Part 1 Phys ical Layer Specification V3.01 Final] definitions. Card capacities of non-secure area, and secure area support [Part 3 Security Specification V3.0 Final] specifications.

The SD V 3.0 card has a 9-pin interface, designed to operate at a maximum frequency of 208MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. The Card capacity could be more than 64GB and up to 2TB in the future with ex-FAT file system, which is called SDXC (Extended Capacity SD Memory Card). Secure Digital 3.0 cards are one of the most popula r cards today due to their high performance, good reliability and wide compatibility.

1.2. Flash Management

1.2.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. The card controller applies the BCH ECC Algorithm that can detect and correct errors occur during Read process, ensure data been read correctly, as well as protect data from corruption.

1.2.2. Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

The card provides advanced Wear Leveling algorithm that can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

1.2.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. The card applies an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.4. Pseudo SLC (pSLC) (ultra MLC)

Pseudo SLC can be considered an extended version of MLC. While MLC contains fast and slow pages, pSLC only applies fast pages for programming. The concept of pSLC is demonstrated in the two tables below. The first and second bits of a memory cell represent a fast and slow page respectively, as shown in the left table. Since only fast pages are programmed when applying pSLC, the bits highlighted in red are used, as shown in the right table. Accordingly, because only fast pages are programmed, pSLC provides better performance and endurance than MLC. Moreover, pSLC performs similarly with SLC, yet pSLC is more cost-effective.

MLC Flash	
1st Bit (Fast)	2nd Bit (slow)
1	1
1	0
0	1
0	0

Pseudo SLC Flash	
1st Bit (Fast)	2nd Bit (slow)
1	1
1	0
0	1
0	0

Figure 1-1 Cell Content of MLC (Left) and Pseudo SLC (Right)

2. PRODUCT SPECIFICATIONS

- **Capacity**

  16GB

- **Support SD system specification version 3.0**
- **Card capacity of non-secure area and secure area support [Part 3 Security Specification Ver3.0 Final] Specifications**
- **Support SD SPI mode**
- **Designed for read-only and read/write cards**
- **Bus Speed Mode (use 4 parallel data lines)**
  - **Non-UHS mode**

    - Default speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5 MB/sec

    - High speed mode: 3.3V signaling, frequency up to 50MHz, up to 25 MB/sec

- **UHS mode**
  - SDR12: SDR up to 25MHz, 1.8V signaling
  - SDR25: SDR up to 50MHz, 1.8V signaling
  - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
  - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

  Note:

  1. Timing in 1.8V signaling is different from that of 3.3V signaling.
  2. To properly run the UHS mode, please ensure the device supports UHS-I mode.

  - **The command list supports [Part 1 Physical Layer Specification Ver3.1 Final] definitions**

    Copyrights Protection Mechanism

    Compliant with the highest security of DPRM standard

    Supports CPRM (Content Protection for Recordable Media) of SD Card

    Card removal during read operation will never harm the content

    Password Protection of cards (optional)

    Write Protect feature using mechanical switch

    Built-in write protection features (permanent and temporary)

  - **Electrostatic Discharge (ESD)**

    ESD protection in pads(contact discharge).

    ESD protection in non-contact pad area(air discharge).

- **Operation voltage range: 2.7 ~ 3.6V**
- **Support Dynamic and Static Wear Leveling**

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

Temperature and Humidity

- Temperature Range (NOTE)
  Operational: -25°C ~ 85°C
  Storage: -25°C ~ 85°C

NOTE: We suggest that customer uses SD/micro SD card during the temperature range for better reliability.

Humidity
Operational: RH = 95% under 25°C
Diamond grade: RH = 93% under 40°C

Table 3-1 High Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	85°C	0% RH	96 hours
Storage	85°C	0% RH	500 hours

Table 3-2 Low Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	-25°C	0% RH	96 hours
Storage	-40°C	0% RH	168 hours

Table 3-3 High Humidity Test Condition

	Temperature	Humidity	Test Time
Operation	25°C	95% RH	1 hours
Storage	40°C	95% RH	500 hours

Table 3-4 Temperature Cycle Test

	Temperature	Test Time	Cycle
Operation	-25°C	30 min	10 Cycles
	85°C	30 min	

Shock

Table 3-5 Shock Specification

	Acceleration Force	Half Sin Pulse Duration
Industrial SD card	1500G	0.5ms

Vibration

Table 3-6 Vibration Specification

	Condition		Vibration Orientation
	Frequency/Displacement	Frequency/Acceleration	
SD card	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G	Direction: X, Y, Z axis/30 min for each

Drop

Table 3-7 Drop Specification

	Height of Drop	Number of Drop
Industrial SD card	150cm free fall	6 face of each unit

Bending

Table 3-8 Bending Specification

	Force	Action
Industrial SD card	≥ 10N	Hold 1min/5times

Torque

Table 3-9 Torque Specification

	Force	Action
Industrial SD card	0.15N-m or +/-2.5 deg	Hold 30 seconds/5times

Switch Cycle Test

Table 3-10 Switch Cycle Test Specification

	Force	Number of Switch Cycle
SD card	0.4N-m~5N-m	1,000 cycles

Durability Mating Cycle Test

Table 3-11 Mating Cycle Test Specification

	Number of Mating Cycle
SD card	10,000 cycles

Electrostatic Discharge (ESD)

Table 3-10 Contact ESD Specification

	Condition	Result
SD card	Contact: +/- 4KV each item 5 times Air: +/- 15KV 5 times	PASS

EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

4. SD CARD COMPARISON

Table 4-1 Comparing SD3.0 Standard, SD3.0 SDHC and SD3.0 SDXC

	SD3.0 Standard (Backward compatible to 2.0 host)	SD3.0 SDHC (Backward compatible to 2.0 host)	SD3.0 SDXC
File System	FAT 12/16	FAT32	exFAT
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support	Support
CMD8 (SEND_IF_COND)	Support	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Support	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support	Not Support
Supply Voltage 2.7v – 3.6v (for initialization)	Support	Support	Support
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

Table 4-2 Comparing UHS Speed Grade Symbols

	U1 (UHS Speed Grade 1)	U3 (UHS Speed Grade 3)
Operable Under	*UHS-I Bus I/F, UHS-II Bus I/F	
SD Memory Card	SDHC UHS-I and UHS-II, SDXC UHS-I and UHS-II	
Mark		
Performance	10 MB/s minimum write speed	30 MB/s minimum write speed
Applications	Full higher potential of recording real-time broadcasts and capturing large-size HD videos.	Capable of recording 4K2K video.

*UHS (Ultra High Speed), the fastest performance category available today, defines bus-interface speeds up to 312 Megabytes per second for greater device performance. It is available on SDXC and SDHC memory cards and devices.

5. ELECTRICAL SPECIFICATIONS

5.1. Power Consumption

The table below is the power consumption.

Table 5-1 Power Consumption

Bus Speed Mode		Max. Power Up Current (uA)	Max. Standby Current (uA)	Max. Read Current (mA)	Max. Write Current (mA)
Default Speed Mode		250	1000	150 @ 3.6V	150 @ 3.6V
High Speed Mode		250	1000	200 @ 3.6V	200 @ 3.6V
UHS-I Mode	UHS50/DDR50	250	1000	400 @ 3.6V	400 @ 3.6V
	UHS104	250	1000	400 @ 3.6V	400 @ 3.6V

NOTES:
1. Power consumptions are measured at room temperature (25C). Standby current might rise to 1600 under 85C
2. Power consumption of Max. Standby Current is for SD cards under and including 64GB only. For 128GB and 256GB, the power consumption is to be determined.

5.2. DC Characteristic

5.2.1. Bus Operation Conditions for 3.3V Signaling

Table 5-2 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	IOH=-2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	IOL=2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3 V		
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Table 5-3 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 5-4 Threshold Level for 1.8V Signaling

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	Vss-0.3	0.58	V	

Table 5-5 Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

5.2.2. Bus Signal Line Load

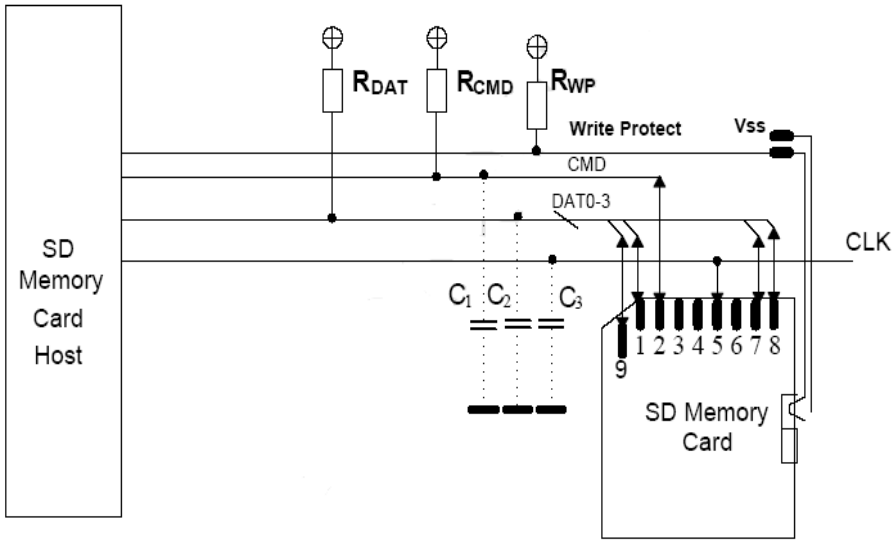


Figure 5-1 Bus Circuitry Diagram

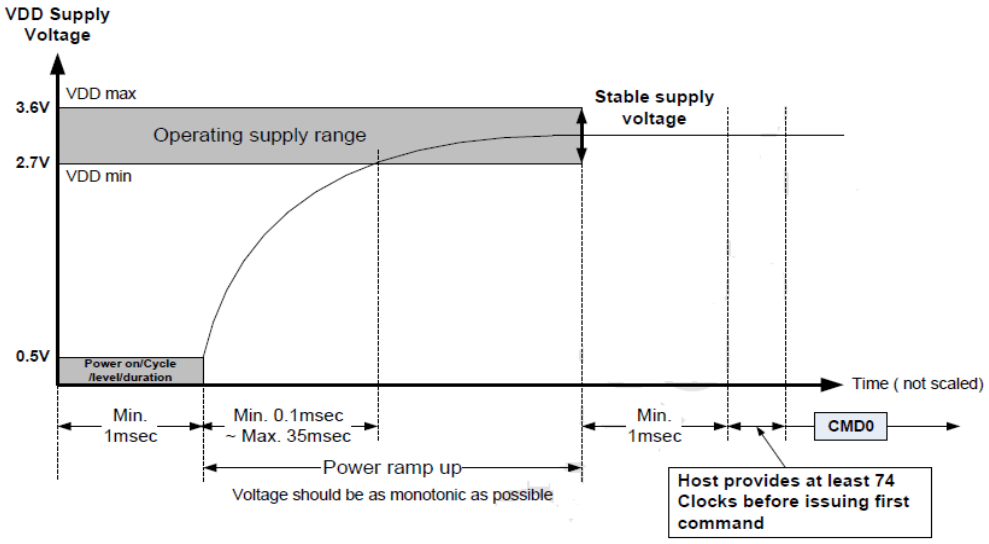
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{CARD}

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1card C_{HOST}+C_{BUS} shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10[1]	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

5.2.3. Power Up Time

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V.

(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendations of Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

(4) Host shall wait until VDD is stable.

(5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

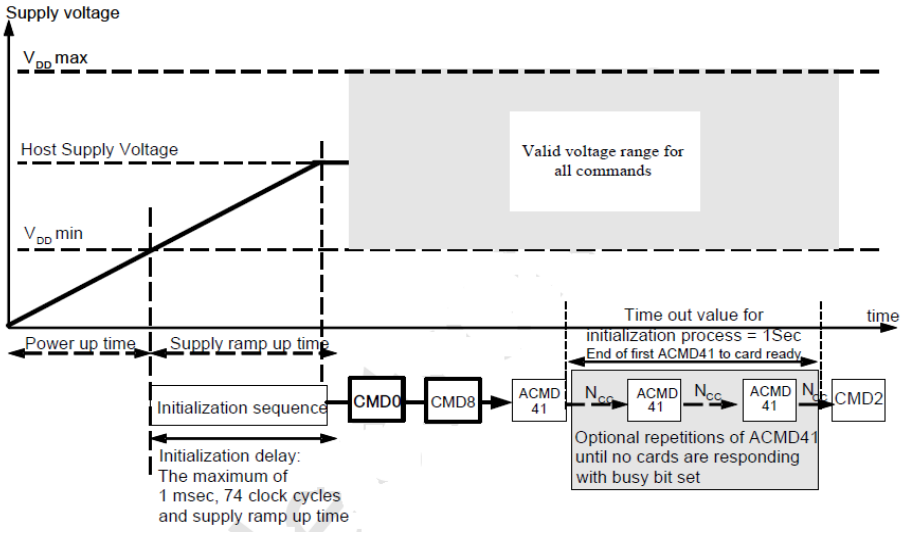
Power Down and Power Cycle

1. When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

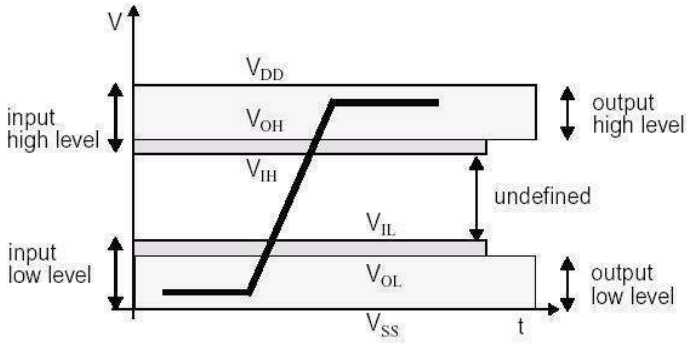
2. If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

5.2.4. Power Up Time of Card

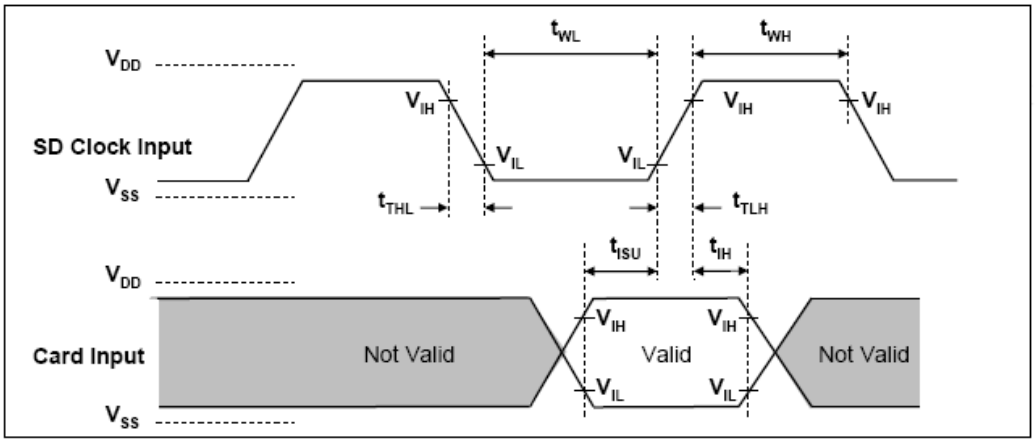
A device shall be ready to accept the first command within 1ms from detecting VDD min.
Device may use up to 74 clocks for preparation before receiving the first command.



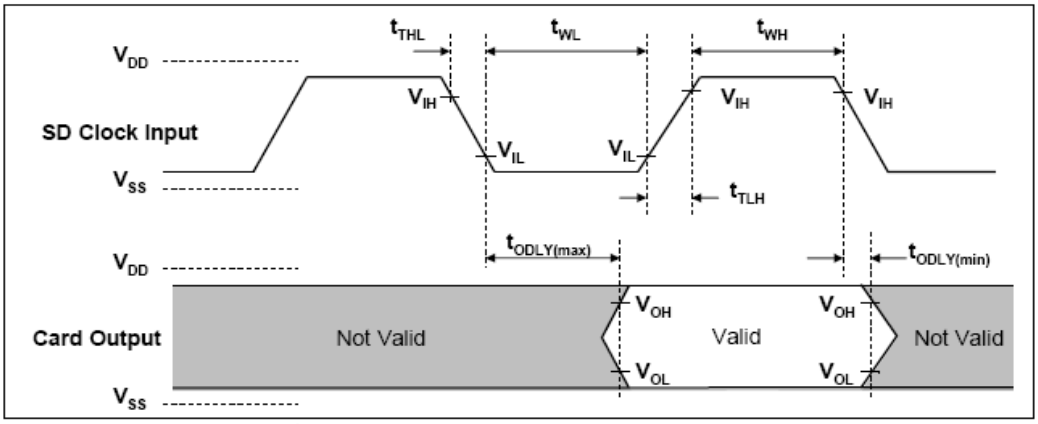
5.3. AC Characteristic



5.3.1. SD Interface Timing (Default)



Card Input Timing (Default Speed Card)

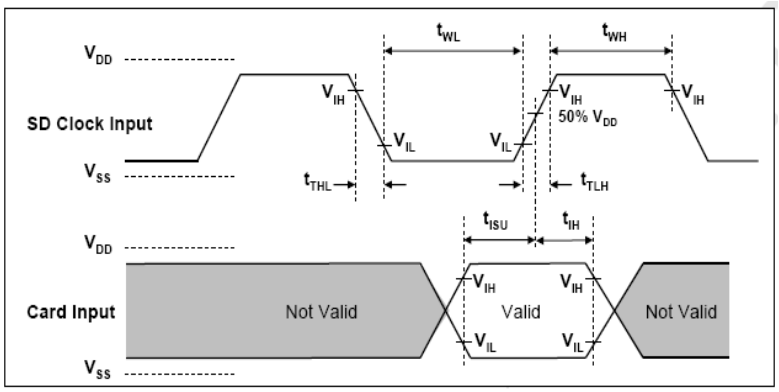


Card Output Timing (Default Speed Mode)

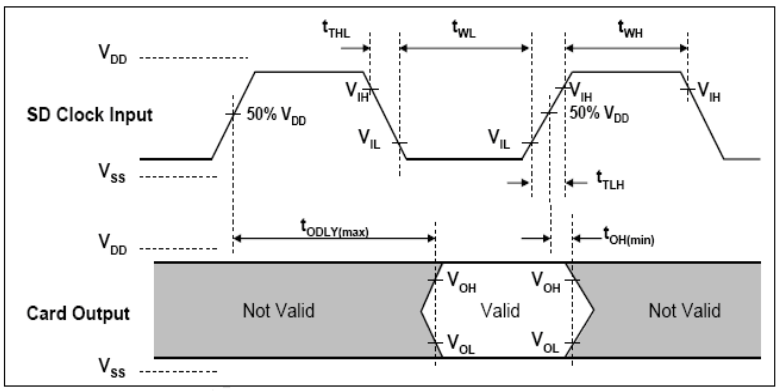
Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(VIH) and max(VIL)					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	Ccard≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	kHz	Ccard≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	Ccard≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	Ccard≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	Ccard≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	Ccard≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	Ccard≤ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	Ccard≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	CL≤40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	CL≤40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

5.3.2. SD Interface Timing (High-Speed Mode)



Card Input Timing (High Speed Card)

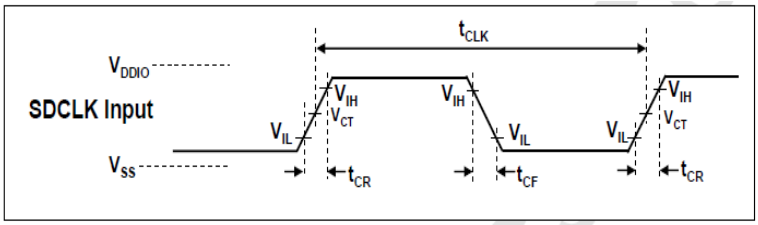


Card Output Timing (High Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(VIH) and max(VIL)					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	Ccard ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	Ccard ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	Ccard ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	Ccard ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	Ccard ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	Ccard ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	Ccard ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	CL ≤ 40 pF (1 card)
Output Hold time	T_{OH}	2.5		ns	CL ≤ 15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

5.3.3. SD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes)

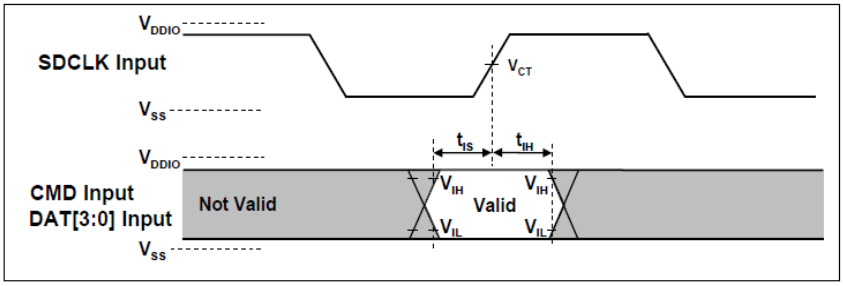


Clock Signal Timing

Table 5-6 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
tCLK	4.80	-	ns	208MHz (Max.), Between rising edge, VCT= 0.975V
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 0.96ns (max.) at 208MHz, CCARD=10pF tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF The absolute maximum value of tCR, tCF is 10ns regardless of clock frequency
Clock Duty	30	70	%	

SDR50 and SDR104 Input Timing

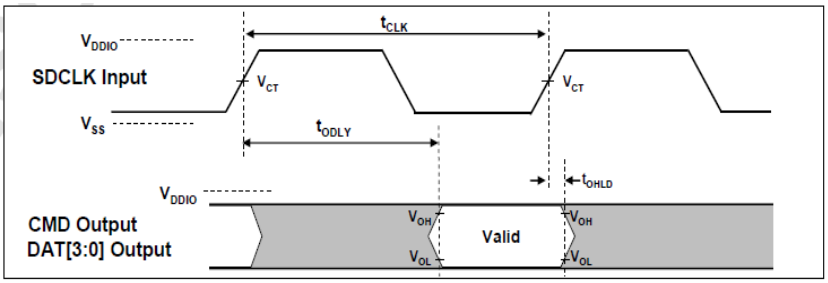


Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
tIS	1.40	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.81	-	ns	CCARD = 5pF, VCT= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
tIS	3.00	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.81	-	ns	CCARD = 5pF, VCT= 0.975V

<Note 1> PS8210 is SD and eMMC(4.51) controller, so the maximum CCARD becomes 12pF and minimum of tIH will be 1.10 ns.

Output(SDR12, SDR25, SDR50)



Output Timing of Fixed Data Window

Table 5-7 Output Timing of Fixed Data Window (SDR12, SDR25, SDR50 Modes)

Symbol	Min	Max	Unit	Remark
tODLY	-	7.5	ns	tCLK>=10.0ns, CL=30pF, using driver Type B, for SDR50
tODLY	-	14	ns	tCLK>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
TOH	1.5	-	ns	Hold time at the tODLY (min.), CL=15pF

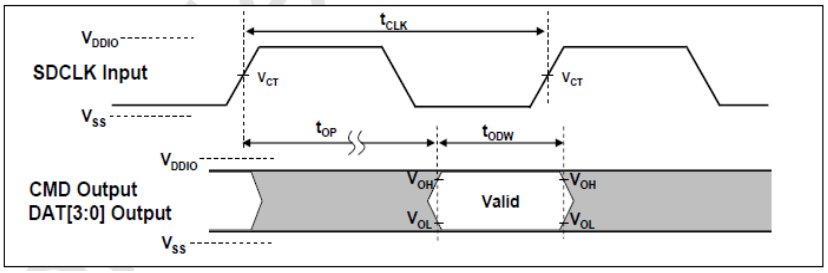
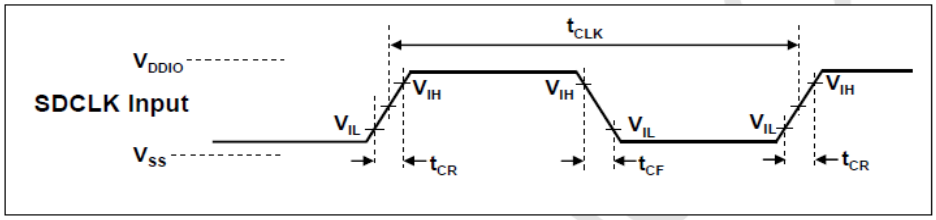


Table 5-8 Output Timing of Variable Window (SDR104)

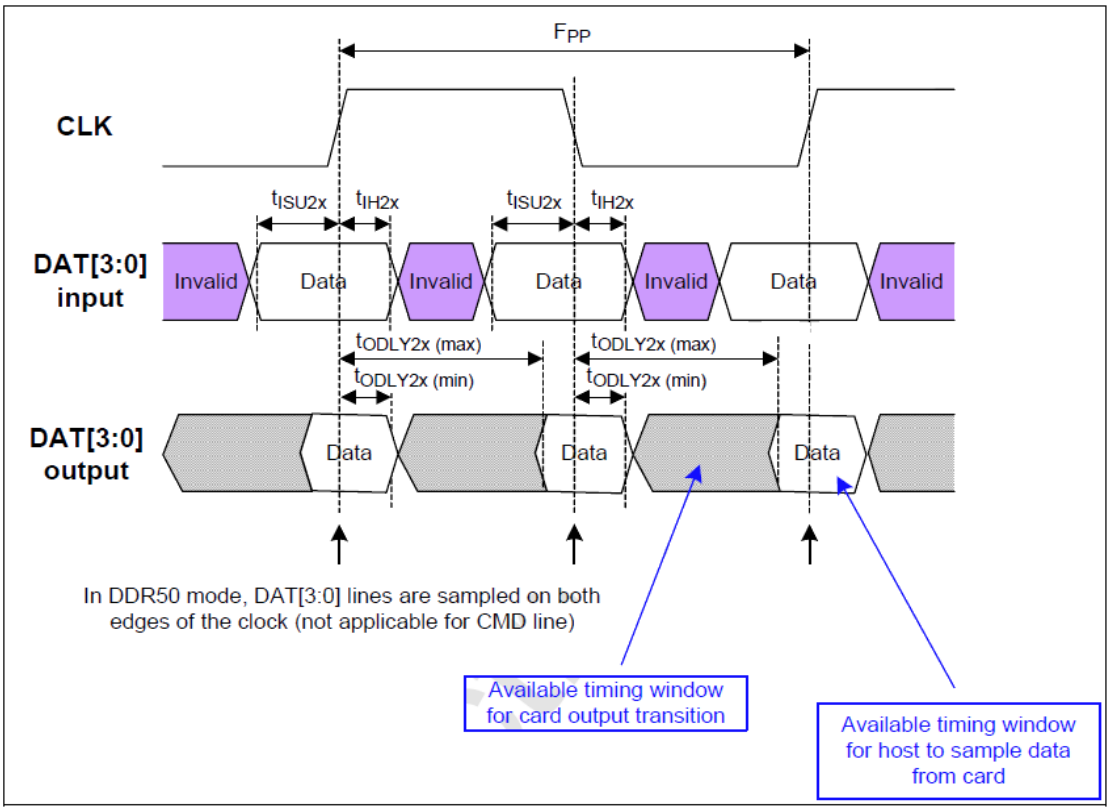
Symbol	Min	Max	Unit	Remark
tOP	0	2	UI	Card Output Phase
Δ tOP	-350	+1550	ps	Delay variable due to temperature change after tuning
tODW	0.60	-	UI	tODW = 2.88ns at 208MHz

5.3.4. SD Interface Timing (DDR50 Mode)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Table 5-8 Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥15 pF (1 card)

6. INTERFACE

6.1. Pad Assignment and Descriptions

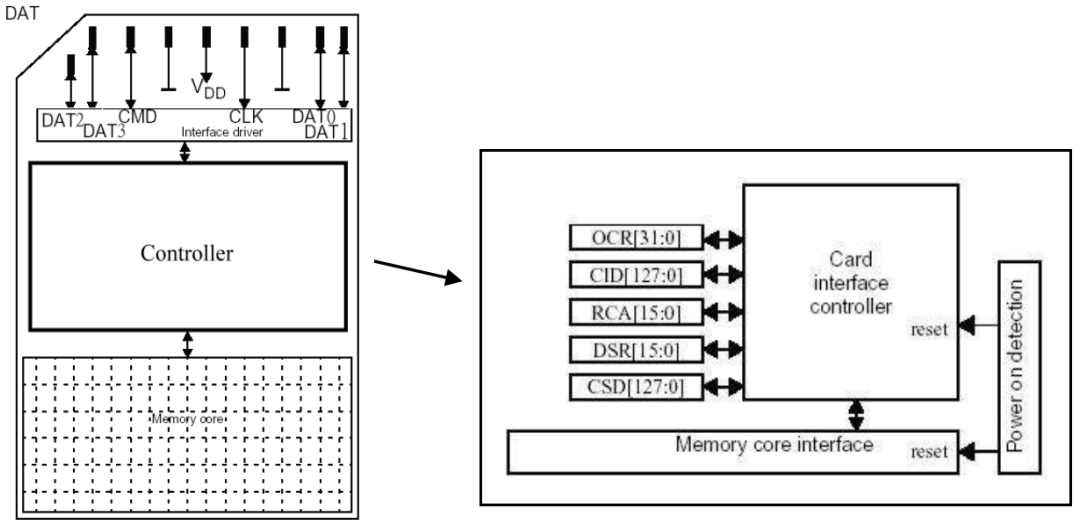


Table 6-1 SD Memory Card Pad Assignment

pin	SD Mode			SPI Mode		
	Name	Type1	Description	Name	Type	Description
1	CD/DAT3 [2]	I/O/PP [3]	Card Detect/Data Line[bit3]	CS	I[3]	Chip Select (net true)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	V_{SS2}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		
9	DAT2	I/O/PP	Data Line[bit2]	RSV		

1. S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers.
2. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode as well while they are not used. It is defined so in order to keep compatibility to MultiMedia Cards.
3. At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA1	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities. **Mandatory**
OCR	32bit	Operation conditions register. **Mandatory**.
SSR	512bit	SD Status; information about the card proprietary features. **Mandatory**
OCR	32bit	Card Status; information about the card status. **Mandatory**

(1) RCA register is not used (or available) in SPI mode.

7. PHYSICAL DIMENSIONS

Dimensions:3 2mm(L) x 24mm(W) x 2.1mm(H)